Reply to initial office action on application number 10/801,431

The following is a response to the USPTO action dated 3/19/05. The italic text is quoted directly from the action document. The text immediately after the italic text is the inventors' response to the specific point made by the examiner.

Information disclosure statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

As requested, the references cited in the application have been separately listed on the attached document.

Claim Rejections- 35 USC 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112: [Quote omitted for brevity]

2. Claims 4 and 5 are rejected under 35 U.S.C 112, first paragraph, as failing to comply with enablement requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

2.a. In re claims 4 and 5, the specification does not disclose "over-layers of other semiconductors specific to the devices fabricated."

The "over-layers" of other semiconductors indicated in the application are device-specific semiconductors. They are in the general category of III-V semiconductors, but their specific details will correspond to whether HEMT devices, MESFETS, bipolar, or other devices are being build in the associated technology. Since their specific details are known to those skilled in the art, and not relevant to the invention, no attempt has been made to list examples of such details.

Claim Rejections - 35 USC 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C 102 that form the basis for the rejections under this section made in this Office action: [Quote omitted for brevity]

Claims 1-5 and 8 are rejected under 35 U.S.C 102(e) as being anticipated by Deshpande et. al. (US 2004/0242010 A1.

In re claim 1, Deshpande (esp. Fig. 3E) discloses a structure providing anneal cap, ion implant mask (68), and shallow trench isolation (70) features for III-V devices comprising a trench etched into the semiconductor, a combination anneal cap/CMP stop layer, and a dielectric trench fill layer, with significant topography reduction compared to the traditional dielectric structure.

In the cited reference, Deshpande actually discloses a method for bird's beak reduction in Si MOS devices. Fig. 3E, and related figures, do not illustrate the final structure formed in fabricating the device, only a simplified view of the structure at an early part of the process. While in paragraph [0061] of the cited reference Deshpande mentions an oxide liner as an optional step, there will be further oxidation of the silicon surface during the subsequent thermal oxidation steps whether or not the structure started with this liner. Because Deshpande has clearly stated the invention is "a method for modifying stress formation..." resulting from bird's beak creation, a layer formed by thermally oxidizing the semiconductor must necessarily be present. Such a layer is not shown in figure 3E, possibly because Deshpande is not claiming the final structure, only a process for reducing the bird's beak. No layer caused by the thermal oxidation of a semiconductor is part of the present invention, so the structure can not be the same as that resulting from Deshpande's method.

In fact, the complete process Deshpande discloses, when including the necessary thermal oxidation, is incompatible with III-V semiconductor devices. The bird's beak phenomenon and resulting active area stress Deshpande invention reduces cannot occur in III-V devices because they have no stable native thermal oxide, so no thermal oxidations are performed in their fabrication. The final structure of Deshpande's invention, as well as every other trench isolation structure that has been previously taught, includes a thermal oxidation layer in contact with at least a part of the semiconductor.

I see nowhere in Deshpande's application any claims to a structure providing anneal cap capabilities. In fact, the final structure built with his method, including the thermal oxide layer grown from the semiconductor substrate, is likely to be a poor anneal cap. Si MOS devices, which Deshpande's invention clearly targets, have no need for an anneal cap. The purpose of an anneal cap is to maintain compound semiconductor stoichiometry when one of the components has significant vapor pressure at anneal temperatures. For example, in the case of GaAs, at anneal temperatures the vapor pressure of arsenic becomes large enough for the semiconductor to lose it's arsenic content at the surface. The anneal cap keeps the arsenic from diffusing out.

In re claims 2, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is GaAs (section [0038).

It is unlikely Deshpande has confirmed the applicability to GaAs and other III-V semiconductors. Given GaAs has no stable native thermal oxide, III-V semiconductor device manufacturing carefully avoids thermal oxidation, and there will be no resulting bird's

beak to fix, it is not clear why anyone who actually understood III-V semiconductor manufacturing would make such a statement.

Whether or not Deshpande's invention are actually applicable to GaAs and other III-V devices is inconsequential, since as shown in the response to claim 1 objections above, the structure is not the same as that claimed in the present invention.

In re claims 3, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is InP (section [0038]).

Whether or not Deshpande's invention are actually applicable to InP and other III-V devices is inconsequential, since as shown in the response to claim 1 objections above, the structure is not the same as that claimed in the present invention

In re claim 4, as best understood, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is GaAs with over-layers of other semiconductors specific to the devices fabricated {As described in sections [0069-0071], the device will be used in combination with various PFET and NFET devices, which will comprise over-layers of semiconductor, such as gate polysilicon layer, as well known in the art}

Claim 4 allows for over-layers of other semiconductors on the substrate. It is well known in the art, that over-layers of doped semiconductors are often grown epitaxially on a substrate to achieve different devices. For example, consecutive layers of n-type GaAs, p-type GaAs, n-type InGaP, and n-type InGaAs are grown on a substrate to achieve bipolar transistors. Different layers could be grown to achieve MESFET or HEMT devices. A gate polysilicon layer is **not** an example of a semiconductor over-layer grown on the substrate material to make up the "III-V semiconductor" of the invention.

In re claim 5, as best understood, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is InP with over-layers of other semiconductors specific to the devices fabricated {As described in sections [0069-0071], the device will be used in combination with various PFET and NFET devices, which will comprise over-layers of semiconductor, such as gate polysilicon layer, as is well known in the art}

Claim 5 allows for over-layers of other semiconductors on the substrate. It is well known in the art, that over-layers of doped semiconductors are often grown epitaxially on a substrate to achieve different devices. For example, consecutive layers of n-type InP, p-type InGaAs, n-type InP, and n-type InGaAs are grown on a substrate to achieve bipolar transistors. Different layers could be grown to achieve MESFET or HEMT devices. A gate polysilicon layer is **not** an example of a semiconductor over-layer grown on the substrate material to make up the "III-V semiconductor" of the invention.

In re claim 8, Deshpande discloses the device of claim 1, wherein said dielectric trench fill layer is silicon dioxide (section [0061]).

Claim 8 discloses silicon dioxide as one of the materials of the structure. This material is the most widely used dielectric in semiconductor fabrication. It has been claimed as a necessary part of thousands of inventions. This is the preferable material for the indicated part of the present invention. Since it has been shown above that the resulting

structure from Deshpande's invention is not the same as the present invention, the fact that both inventions use silicon dioxide should not be grounds for rejection of this claim.

Claim Rejections - 35 USC 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: [Quote omitted for brevity]

4. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deshpande et. al. as applied to claim 1 above, and further in view of Ohta (US 2004/ 0126990A1).

In re claim 6, Deshpande discloses the device of claim 1, but does not expressly disclose the silicon nitride layer being in the range of 100 to 3000 angstroms. Ohta discloses a silicon nitride liner having a thickness of 20 to 40 nm, which equates to 200 to 400 angstroms. It would have been obvious for one skilled in the art at the time of the invention to use a thicker liner layer as disclosed by Ohta for the device of Deshpande for the purpose, for example, of enhancing FET characteristics, such as increased drain current, by generating greater tensile stress in the silicon nitride layer (Ohta; sections [0032, 0045, 0056]).

In re claim 7, Deshpande discloses the device of claim 1. Ohta discloses a silicon nitride liner having a thickness of 20 to 40 nm, which equates to 2 to 4 percent of the trench depth. Deshpande discloses the claimed invention wherein the trench depth is in the range of 1 μm (1000nm), section [0047], but does not expressly disclose the silicon nitride layer having a thickness of 5 to 25 percent of the trench depth. It would have been obvious to one having ordinary skill in the art at the time the invention was made to increase the thickness of the nitride liner since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ223. To do so would improve the FET characteristics, such as drain current, as disclosed by Ohta (sections [0032, 0045, 0056]).

As established in the above discussion directed specifically at claim 1, Deshpande does not disclose the device of claim 1 as previously assumed. Claims 6 and 7 specify utilization of silicon nitride. Silicon nitride is the second most widely used dielectric in semiconductor manufactureing.It has been claimed as a necessary part of thousands of patents. It's use in previous inventions with different purposes and structures should not preclude its use in the present invention with a new purpose and structure.

The purpose of the current invention is not, as indicated, to enhance "FET characteristics, such as increased drain current, by generating greater tensile stress in the silicon nitride layer" (by reducing the divot). In simple terms, Ohta's invention is specifically intended to reduce the divot formed with certain STI MOS processes. The problem Ohta is fixing is associated with thermal oxidation processes, and is not an issue with III-V semiconductors.

The purpose of disclosing the nitride thickness as a function of the trench depth is related to the integrated CMP stop capabilities of the invention. While nitride thickness

has a secondary influence on anneal cap capabilities, it has a primary influence on CMP stop capabilities. Since there are advantages in using a single nitride layer for all aspects of the invention, the thickness has been specified as indicated. Note that the factors determining the nitride thickness of Deshpande's and Ohta's inventions will be completely different, and are related to the ability of the nitride layer to slow oxide growth in the underlying silicon. There is no such issue in III-V semiconductors because of the lack of a thermal oxidation step in processing such semiconductors.

Perhaps some of the confusion on Ohta's device comes from the wording in his claim 5, where the structure, "...an isolation trench formed under a surface of said semiconductor substrate..." includes both an impression etched into the substrate **and** an oxide liner. This oxide liner is listed as layer 7 in all of his figures. However, even if Ohta had left out the layer 7 in his figures, a thermal oxide layer of some type would have to be implied in his invention because the problem he is clearly fixing is the result of a thermal oxidation.

David A. Johnson 6-6-05